Phani Jayanth Jonnalagadda

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EDUCATION

ETH Zürich Zürich, Switzerland

M.Sc. Electrical Engineering (Computers & Networks): **CGPA N/A** (Sep 2023 - Present)

Relevant Coursework: Computer Architecture, VLSI 1,2 & 4, Embedded Systems, Machine Learning on Microcontrollers, Systems-on-Chip for Data Analytics and Machine Learning, Synthesis of Digital Circuits

Indian Institute of Technology Madras (IITM) Chennai, India

B.Tech. in Electrical Engineering & Minor in Computing: **CGPA 9.1/10** (Jul 2019 - Jun 2023)

Relevant Coursework: Computer Architecture, Hardware Security, Digital IC Design, Digital Systems, Testing & Testable Design, Modeling and Optimization in VLSI, Mapping Algorithms to Architectures

SKILLS

Languages: System Verilog, Verilog, Bluespec Verilog, Python, C/C++

Tools & Frameworks: Gem5, ChampSim, Synopsys, Questasim, Verilator, LTSpice, Spike, GNU Electric

Others: PyTorch, CUDA, Git, Docker, LaTeX, STM, RPi, Arduino Embedded Devices

PROJECTS

A RISC-V ISA Extension for Scalar Chaining in Snitch[ɻ]

Semester Thesis, Prof. Dr. Luca Benini, ETH Zürich (Mar 2024 - Present)

◆ Extending the Snitch Core to hide RAW dependency stalls without increasing the register pressure.
◆ Enabling efficient floating-point computations with comparable performance to vector & OoO engines.

Traffic Image Segmentation on Edge

Course Project, Machine Learning on Microcontrollers, ETH Zürich (Nov 2023 - Jan 2024)

◆ Implemented U-Net-based traffic image segmentation on the STM32M4 and MAX78000 edge devices.
◆ Achieved ~90% mIoU score across 4 segmentation classes through QAT on the MAX78000 board.

RISC-V Vector ISA Support in SHAKTI[$]

Undergraduate Thesis, Prof. Kamakoti V, IITM (Nov 2022 - May 2023)

◆ Engineered configurable Vector Functional Units in Bluespec System Verilog for the SHAKTI C-Class[$].

In-Memory Computing (IMC) Engine

Course Project, Embedded Memory Design, IITM (Apr 2022 - Jun 2022)

◆ Designed an SRAM-based IMC engine that performs MAC operations using GNU Electric and LTSpice.

Acceleration of Static Mandelbrot Fractal Image Generation (Apr 2022 - May 2022)

◆ Accelerated the generation of Mandelbrot fractals on an Artix 7 FPGA using Vivado HLS and Verilog.

Acceleration of Advanced Encyrption Standard (AES) Algorithm (Dec 2021)

◆ Accelerated AES (35X over a 2.9GHz PC) in Verilog and performed the entire RTL to GDSII flow.

PROFESSIONAL EXPERIENCE

Qualcomm, *Hardware Engineering Intern, GPU Design Team* *Bengaluru, India (May - Aug 2022)*

◆ Developed a Python-based framework for identifying redundant retention flops in the GPU subsystem.
◆ Utilized PrimeTime(PX) from Synopsys to obtain the potential redundancies for power curtailment.

LEADERSHIP & TEACHING EXPERIENCE

Core Member, Electronics Club, CFI[&], IITM (Apr 2020 - Apr 2022)

◆ Spearheaded a 3-Tier Team of 50+ electronics enthusiasts and managed events and sessions.
◆ Conducted workshops on Parallel Programming, CUDA, and RTOS for 100+ participants.

ɻ github.com/pulp-platform/snitch_cluster $ India's first indigenous RISC-V Microprocessor (shakti.org.in) & Centre for Innovation (India's Largest Student-Run Research Lab at IITM)